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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/517,462

**Applicant(s)**

PETTENDORF ET AL.

**Examiner**

Syed Bokhari

**Art Unit**

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on 08 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 and 21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 and 21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 12/06/2004.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 101***

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 21 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention is not directed to process, a machine, manufacturer, or composition of matter, or any new and useful improvement thereof. Claim 21 is drawn to a program for executing data communication control processing. There must be some connection between the computer program instruction and the physical device executing the instructions through a computer-readable medium that meets the statutory requirements as set forth in the guidelines in MPEP 2106.01 [R-6].

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-2, 7-9, 12-13 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (USP 6,512,753 B1) in view of Eo et al. (USP 6,069,574).

Kim et al. discloses an Orthogonal Variable Spreading Factor (OVSF) generator with the following features: regarding claim 1, a code generator for generating an orthogonal code having a spreading factor (SF) and an index (k) (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "a spreading code index- k is the input to a spreading code generator 740" recited in column 6 lines 9-11),

wherein the spreading factor (SF) is selectable from values in a range  $1 < SF < \text{or } = SF_{\text{max}}$  with  $SF_{\text{max}}$  denoting a maximum spreading factor (Fig. 5, spreading symbols of different lengths using spreading codes of same length, see "in 1x system the spreading factor range is 1-128 whereas in 3x system the range is 1-256" recited in column 5 lines 45-59) and the code generator comprising an index conversion unit for converting the index (k) into a modified index (j) associated with a corresponding code having the maximum spreading factor (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "upon receipt of the spreading code index-k, an index controller 742 outputs a mask index and a walsh orthogonal code index" recited in column 6 lines 13-25); regarding claim 2, wherein the corresponding code is one of: an orthogonal variable spreading factor (OVSF) code, a Hadamard code, and a Walsh code (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "adder 748 adds quasi-orthogonal mask and the Walsh orthogonal code from Walsh orthogonal code 746, to generate a quasi-orthogonal code" recited in column 6 lines 25-37); regarding claim 12, a method of generating an orthogonal code having a spreading factor (SF) and an index (k) (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "a spreading code index- k is the input to a spreading code generator 740" recited in column 6 lines 9-11), wherein the spreading factor (SF) is selectable from values in a range  $1 < SF < \text{or } = SF_{\text{max}}$ , with  $SF_{\text{max}}$  denoting a maximum spreading factor (Fig. 5, spreading symbols of different lengths using spreading codes of same length, see "in 1x system the spreading factor range is 1-128 whereas in 3x system the range is 1-256" recited in column 5 lines 45-59), the

method comprising the steps of converting the index (k) into a modified index (j) associated with a corresponding code having the maximum spreading factor (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "upon receipt of the spreading code index-k, an index controller 742 outputs a mask index and a walsh orthogonal code index" recited in column 6 lines 13-25), and regarding claim 13, wherein the corresponding code is one of: an orthogonal variable spreading factor (OVSF) code, a Hadamard code, and a Walsh code (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "adder 748 adds quasi-orthogonal mask and the Walsh orthogonal code from Walsh orthogonal code 746, to generate a quasi-orthogonal code" recited in column 6 lines 25-37).

Kim et al. does not disclose the following features: regarding claim 1, a logic unit for performing logic operations on bits of the modified index (j) and bits of a counter value (i), thereby generating a code bit of the orthogonal code; regarding claim 7, wherein the logic unit includes: adding means for performing binary AND operations, wherein the adding means is adapted to receive a bit of the modified index (j) and a bit of the counter value (i), and is further adapted to output a binary output value representing a binary AND combination of the two bits; and combining means for combining the binary output values into the code bit; regarding claim 8, wherein the combining means includes means for performing binary XOR operations; regarding claim 9, further comprising a counter for generating the counter value (i); regarding claim 12, initializing a counter, value (i); c) performing logic operations on bits of the modified index (j) and bits of the counter value (i), thereby generating a code bit of the

orthogonal code; d) incrementing the counter value (i) by one; and e) repeating steps c) and d) until a desired number of code bits has been generated; regarding claim 18, includes the steps of: performing binary AND operations, wherein each operation is adapted to combine a bit of the modified index (j) and a bit of the counter value (i), and to output a binary output value representing a binary AND combination of the two bits; and combining the binary output values into the code bit and regarding claim 19, wherein the step of combining includes performing binary XOR operations.

Eo et al. discloses a Hadamard code generation circuit with the following features: regarding claim 1, a logic unit for performing logic operations on bits of the modified index (j) and bits of a counter value (i) (Fig. 1, a circuit for generating Hadamard codes, see "two AND gates 118 and 119 receive output signal from the counter 112 and index bit from the register 114" recited in column 1 lines 41-44), thereby generating a code bit of the orthogonal code (Fig. 1, a circuit for generating Hadamard codes, see "a XOR gate 124 hereby generating a Hadamard code" recited in column 1 lines 44-46); regarding claim 7, wherein the logic unit includes adding means for performing binary AND operations (Fig. 1, a circuit for generating Hadamard codes, see "final Hadamard code is generated through a binary addition operation at AND gate" recited in column 1 lines 58-63), wherein the adding means is adapted to receive a bit of the modified index (j) and a bit of the counter value (i), and is further adapted to output a binary output value representing a binary AND combination of the two bits (Fig. 1, a circuit for generating Hadamard codes, see "two AND gates 118 and 119 receive output signal from the counter 112 and index bit from the register 114" recited in column

1 lines 41-44); and combining means for combining the binary output values into the code bit (Fig. 1, a circuit for generating Hadamard codes, see "a XOR gate 124 hereby generating a Hadamard code" recited in column 1 lines 44-46); regarding claim 8, wherein the combining means includes means for performing binary XOR operations (Fig. 1, a circuit for generating Hadamard codes, see "a XOR gate 124 hereby generating a Hadamard code" recited in column 1 lines 44-46); regarding claim 9, further comprising a counter for generating the counter value (i) (Fig. 1, a circuit for generating Hadamard codes, see "the value of selecting the output signal from the counter is determined by an index stored in register" recited in column 1 lines 63-65); regarding claim 12, initializing a counter, value (i) (Fig. 8, circuit for generating Hadamard code, see "the counter 81 is initialized by init-rest signal" recited in column 13 lines 66-67 and column 14 lines 59-60), performing logic operations on bits of the modified index (j) and bits of the counter value (i) (Fig. 1, a circuit for generating Hadamard codes, see "two AND gates 118 and 119 receive output signal from the counter 112 and index bit from the register 114" recited in column 1 lines 41-44), thereby generating a code bit of the orthogonal code (Fig. 1, a circuit for generating Hadamard codes, see "a XOR gate 124 hereby generating a Hadamard code" recited in column 1 lines 44-46), incrementing the counter value (i) by one (Fig. 2, a circuit for generating Hadamard codes, see "these values are sequentially outputted" recited in column 7 lines 6-11), until a desired number of code bits has been generated (Fig. 1, a circuit for generating Hadamard codes, see "the value for selecting the output signal from the counter is determined by index stored register for final Hadamard code"



recited in column 1 lines 63-66 and column 2 lines 1-3); regarding claim 18, includes the steps of: performing binary AND operations (Fig. 1, a circuit for generating Hadamard codes, see "final Hadamard code is generated through a binary addition operation at AND gate" recited in column 1 lines 58-63), wherein each operation is adapted to combine a bit of the modified index (j) and a bit of the counter value (i), to output a binary output value representing a binary AND combination of the two bits (Fig. 1, a circuit for generating Hadamard codes, see "two AND gates 118 and 119 receive output signal from the counter 112 and index bit from the register 114" recited in column 1 lines 41-44); and combining the binary output values into the code bit (Fig. 1, a circuit for generating Hadamard codes, see "a XOR gate 124 hereby generating a Hadamard code" recited in column 1 lines 44-46) and regarding claim 19, wherein the step of combining includes performing binary XOR operations (Fig. 1, a circuit for generating Hadamard codes, see "a XOR gate 124 hereby generating a Hadamard code" recited in column 1 lines 44-46).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Kim et al. by using the features, as taught by Eo et al., in order to provide a logic unit for performing logic operations on bits of the modified index (j) and bits of a counter value (i), thereby generating a code bit of the orthogonal code, adding means for performing binary AND operations, wherein the adding means is adapted to receive a bit of the modified index (j) and a bit of the counter value (i), and is further adapted to output a binary output value representing a binary AND combination of the two bits; and combining means for combining the binary output

values into the code bit, combining means includes means for performing binary XOR operations, a counter for generating the counter value (i), initializing a counter, value (i); c) performing logic operations on bits of the modified index (j) and bits of the counter value (i), thereby generating a code bit of the orthogonal code; d) incrementing the counter value (i) by one; and e) repeating steps c) and d) until a desired number of code bits has been generated. The motivation of using these functions is to enhance the system in a cost effective manner.

6. Claims 5-6 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (USP 6,512,753 B1) in view of Eo et al. (USP 6,069,574) as applied to claim 1 and 12 above, and further in view of Kim et al. (USP 6,671,251 B1).

Kim et al. and Eo et al. disclose the claimed limitations as described in paragraph 5 above. Kim et al. and Eo et al. do not disclose the following features: regarding Claim 5, wherein the index conversion unit includes a permutation unit for permuting the bits of the index (k); regarding claim 6, wherein the index conversion unit includes: a permutation unit for permuting the bits of the index (k); and selection means for selecting, depending upon a mode signal indicating a desired type of the orthogonal code, the output of the permutation unit or the output of the shift register, thereby generating the modified index (j); regarding claim 16, wherein step a) includes permuting the bits of the index (k) and regarding claim 17, wherein step a) includes the steps of: permuting the bits of the index (k); and selecting, depending upon a mode

signal indicating a desired type of the orthogonal code, the permuted index or the shifted index, thereby generating the modified index (j).

Kim et al. discloses a communication system for generating complex quasi-orthogonal code for spreading channel data with the following features: regarding claim 5, wherein the index conversion unit includes a permutation unit for permuting the bits of the index (k) (Fig. 5, a procedure for generating complex quasi-orthogonal codes, see "the M-sequence are column permuted with permutation function to generate a Walsh code" recited in column 5 lines 30-35 and column 8 lines 36-45); regarding claim 6, wherein the index conversion unit includes: a permutation unit for permuting the bits of the index (k) (Fig. 5, a procedure for generating complex quasi-orthogonal codes, see "the M-sequence are column permuted with permutation function to generate a Walsh code" recited in column 5 lines 30-35 and column 8 lines 36-45), selection means for selecting, depending upon a mode signal indicating a desired type of the orthogonal code (Fig. 10, complex quasi-orthogonal code generator which generates quasi-orthogonal code mask in number, see "selectively outputs a mask corresponding to quasi-orthogonal code" recited in column 22 lines 12-20), the output of the permutation unit or the output of the shift register, thereby generating the modified index (j) (Fig. 5, a procedure for generating complex quasi-orthogonal codes, see "by circularly shifting M-sequence and column permutating the circularly shifted specific sequences for converting the generated M-sequence to Walsh orthogonal codes" recited in column 2 lines 53-65); regarding claim 16, wherein step a) includes permuting the bits of the index (k) (Fig. 5, a procedure for generating complex quasi-orthogonal

codes, see "the M-sequence are column permuted with permutation function to generate a Walsh code" recited in column 5 lines 30-35 and column 8 lines 36-45) and regarding claim 17, wherein step a) includes the steps of: permuting the bits of the index (k) (Fig. 5, a procedure for generating complex quasi-orthogonal codes, see "the M-sequence are column permuted with permutation function to generate a Walsh code" recited in column 5 lines 30-35 and column 8 lines 36-45), selecting, depending upon a mode signal indicating a desired type of the orthogonal code (Fig. 10, complex quasi-orthogonal code generator which generates quasi-orthogonal code mask in number, see "selectively outputs a mask corresponding to quasi-orthogonal code" recited in column 22 lines 12-20) and the permuted index or the shifted index, thereby generating the modified index (j) (Fig. 5, a procedure for generating complex quasi-orthogonal codes, see "by circularly shifting M-sequence and column permutating the circularly shifted specific sequences for converting the generated M-sequence to Walsh orthogonal codes" recited in column 2 lines 53-65).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Kim et al. by using the features, as taught by Kim et al. in order to provide the index conversion unit includes a permutation unit for permuting the bits of the index (k), the index conversion unit includes a permutation unit for permuting the bits of the index (k), selection means for selecting, depending upon a mode signal indicating a desired type of the orthogonal code, the output of the permutation unit or the output of the shift register, thereby generating the modified index

(j). The motivation of using these functions is to enhance the system in a cost effective manner.

7. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (USP 6,512,753 B1) in view of Eo et al. (USP 6,069,574) and Rabaeijs et al. (USP 6,967,992 B1).

Kim et al. discloses the following features: regarding claim 10, parallel code generator for concurrently generating a number  $p > 1$  orthogonal codes having respective spreading factors ( $SF_{sub.1}$ ,  $SF_{sub.p}$ ) and indices ( $k_{sub.1}$ ,  $k_{sub.p}$ ) (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "a spreading code index-  $k$  is the input to a spreading code generator 740" recited in column 6 lines 9-11), wherein the spreading factor ( $SF$ ), wherein the spreading factors are selectable from values in a range  $1 < SF_1, \dots, SF_p < \text{or} = SF_{max}$ , with  $SF_{max}$  denoting a maximum spreading factor (Fig. 5, spreading symbols of different lengths using spreading codes of same length, see "in 1x system the spreading factor range is 1-128 whereas in 3x system the range is 1-256" recited in column 5 lines 45-59), an index conversion unit for converting the index ( $k$ ) into a modified index ( $j$ ) associated with a corresponding code having the maximum spreading factor (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "upon receipt of the spreading code index- $k$ , an index controller 742 outputs a mask index and a walsh orthogonal code index" recited in column 6 lines 13-25); regarding claim 11, a parallel code generator for concurrently

generating a number  $p > 1$  orthogonal codes having respective spreading factors (SF.1, . . . SF.p) and indices (k..1, .k.p) (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "a spreading code index- k is the input to a spreading code generator 740" recited in column 6 lines 9-11), wherein the spreading factors are selectable from values in a range  $1 < \text{SF.1, .F.p} < \text{or} = \text{SF.max}$ , with SF.max denoting a maximum spreading factor the parallel code generator comprising (Fig. 5, spreading symbols of different lengths using spreading codes of same length, see "in 1x system the spreading factor range is 1-128 whereas in 3x system the range is 1-256" recited in column 5 lines 45-59), a number (p) of code generators, each of the code generators including an index conversion unit for converting the index (k) into a modified index (j) associated with a corresponding code having the maximum spreading factor (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "upon receipt of the spreading code index-k, an index controller 742 outputs a mask index and a walsh orthogonal code index" recited in column 6 lines 13-25).

Kim et al. does not disclose the following features: regarding claim 10, the parallel code generator comprising: a number (p) of code generators, each for generating one of the p orthogonal codes having a particular one of the spreading factors and a particular one of the indices, each of the (p) code generators including and a logic unit for performing logic operations on bits of the modified index (j) and bits of a counter value (i), thereby generating a code bit of the orthogonal code; regarding claim 11, a logic unit for performing logic operations on bits of the modified index (j) and bits of a counter value (i), thereby generating a code bit of the orthogonal code; and a

counter for generating the counter value (i); wherein each of the code generators generates one of the (p) orthogonal codes having a particular one of the spreading factors and a particular one of the indices.

Eo et al. discloses the following features: regarding claim 10, a logic unit for performing logic operations on bits of the modified index (j) and bits of a counter value (i), thereby generating a code bit of the orthogonal code (Fig. 2, orthogonal code generating apparatus, see "the logic unit AND gate 140 operates on bit from the counter 130 and bits from modified index" recited in paragraph 0021 lines 9-18) and a counter for generating the counter value (i) to be used by the (p) code generators (Fig. 2, orthogonal code generating apparatus, see "the logic unit AND gate 140 operates on bit from the counter 130 and bits from modified index" recited in paragraph 0021 lines 9-18); regarding claim 11, a logic unit for performing logic operations on bits of the modified index (j) and bits of a counter value (i), (Fig. 2, orthogonal code generating apparatus, see "the logic unit AND gate 140 operates on bit from the counter 130 and bits from modified index" recited in paragraph 0021 lines 9-18), thereby generating a code bit of the orthogonal code (Fig. 2, orthogonal code generating apparatus, see "XOR gate 150 operates when results from 140 are received and OVSF code is generated" recited in paragraph 0021 lines 18-21) and a counter for generating the counter value (i) (Fig. 2, orthogonal code generating apparatus, see "the logic unit AND gate 140 operates on bit from the counter 130 and bits from modified index" recited in paragraph 0021 lines 9-18).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Kim et al. by using the features, as taught by Eo et al., in order to provide the parallel code generator comprising a number (p) of code generators, each for generating one of the p orthogonal codes having a particular one of the spreading factors and a particular one of the indices, each of the (p) code generators including and a logic unit for performing logic operations on bits of the modified index (j) and bits of a counter value (i), thereby generating a code bit of the orthogonal code, a logic unit for performing logic operations on bits of the modified index (j) and bits of a counter value (i), thereby generating a code bit of the orthogonal code; and a counter for generating the counter value (i); wherein each of the code generators generates one of the (p) orthogonal codes having a particular one of the spreading factors and a particular one of the indices. The motivation of using these functions is to enhance the system in a cost effective manner.

Kim et al. and Eo et al. do not disclose the following features: regarding claim 10, the parallel code generator comprising: a number (p) of code generators, each for generating one of the p orthogonal codes having a particular one of the spreading factors and a particular one of the indices, each of the (p) code generators including and regarding claim 11, wherein each of the code generators generates one of the (p) orthogonal codes having a particular one of the spreading factors and a particular one of the indices.

Rabaeijs et al. discloses a wireless communication technique for operating the components to receive spread spectrum signals with the following features: regarding



claim 10, the parallel code generator comprising a number (p) of code generators, each for generating one of the p orthogonal codes having a particular one of the spreading factors and a particular one of the indices, each of the (p) code generators including (Fig 15, a p code generator, see "the p code generator 92 contains functionality for generating replicas of the p code sequence, p code variables, initializing the p code and perform p code handover" recited in column 20 lines 41-55) and regarding claim 11, wherein each of the code generators generates one of the (p) orthogonal codes having a particular one of the spreading factors and a particular one of the indices (Fig 15, a p code generator, see "the p code generator 92 contains functionality for generating replicas of the p code sequence, p code variables, initializing the p code and perform p code handover" recited in column 20 lines 41-55).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Kim et al. with Eo et al. by using the features, as taught by Rabaeijs et al., in order to provide the parallel code generator comprising a number (p) of code generators, each for generating one of the p orthogonal codes having a particular one of the spreading factors and a particular one of the indices, each of the (p) code generators including and each of the code generators generates one of the (p) orthogonal codes having a particular one of the spreading factors and a particular one of the indices. The motivation of using these functions is to enhance the system in a cost effective manner.

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (USP 6,512,753 B1) in view of Eo et al. (USP 6,069,574) and Schooler et al. (US 2005/0053049 A1).

Kim et al. discloses the following features: regarding claim 21, generate an orthogonal code having a spreading factor (SF) and an index (k), wherein the spreading factor (SF) (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "a spreading code index- k is the input to a spreading code generator 740" recited in column 6 lines 9-11), wherein the spreading factor (SF) is selectable from values in a range  $1 < SF \leq SF_{sub.max}$ , with  $SF_{sub.max}$  denoting a maximum spreading factor (Fig. 5, spreading symbols of different lengths using spreading codes of same length, see "in 1x system the spreading factor range is 1-128 whereas in 3x system the range is 1-256" recited in column 5 lines 45-59), wherein, the following steps are performed: a) converting the index (k) into a modified index (j) associated with a corresponding code having the maximum spreading factor (Fig. 7, a spreading device for a transmitter in a mobile communication system, see "upon receipt of the spreading code index-k, an index controller 742 outputs a mask index and a walsh orthogonal code index" recited in column 6 lines 13-25).

Kim et al. does not disclose the following features: regarding claim 21, a computer program product directly loadable into an internal memory of a communication unit, the product comprising software code portions that when the product is run on a processor of the communication unit, initializing a counter value (i), performing logic

operations on bits of the modified index (j) and bits of the counter value (i), thereby generating a code bit of the orthogonal code, incrementing the counter value (i) by one and repeating steps c) and d) until a desired number of code bits has been generated. Eo et al. discloses the following features: regarding claim 21, initializing a counter value (i) (Fig. 8, circuit for generating Hadamard code, see "the counter 81 is initialized by init-rest signal" recited in column 13 lines 66-67 and column 14 lines 59-60), performing logic operations on bits of the modified index (j) and bits of the counter value (i), (Fig. 1, a circuit for generating Hadamard codes, see "two AND gates 118 and 119 receive output signal from the counter 112 and index bit from the register 114" recited in column 1 lines 41-44), thereby generating a code bit of the orthogonal code (Fig. 1, a circuit for generating Hadamard codes, see "a XOR gate 124 hereby generating a Hadamard code" recited in column 1 lines 44-46), incrementing the counter value (i) by one (Fig. 2, a circuit for generating Hadamard codes, see "these values are sequentially outputted" recited in column 7 lines 6-11) and repeating steps c) and d) until a desired number of code bits has been generated (Fig. 1, a circuit for generating Hadamard codes, see "the value for selecting the output signal from the counter is determined by index stored register for final Hadamard code" recited in column 1 lines 63-66 and column 2 lines 1-3).

Kim et al. and Eo et al. do not disclose the following features: regarding claim 21, a computer program product directly loadable into an internal memory of a communication unit, the product comprising software code portions that when the product is run on a processor of the communication unit.

Schooler et al. discloses a wireless system for a programmable code generator with the following features: regarding claim 21, a computer program product directly loadable into an internal memory of a communication unit, the product comprising software code portions that when the product is run on a processor of the communication unit (Fig. 3, generation of the synchronization channel (SCH), the primary common control physical channel (PCCPCH) and the common pilot channel (CPICH) by a node, see "computer usable medium including a program for generating the code sequence, see, "for selecting a code type, for generating a plurality of instruction and for storing the instruction" recited in paragraph 0021 lines 1-7).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Kim et al. with Eo et al. by using the features, as taught by Schooler et al. et al. in order to provide a computer program product directly loadable into an internal memory of a communication unit, the product comprising software code portions that when the product is run on a processor of the communication unit. The motivation of using these functions is to enhance the system in a cost effective manner.

9. Claims 3-4 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (USP 6,512,753 B1) in view of Eo et al. (USP 6,069,574) as applied to claim 1 above, further in view of Piccinonno (WO 01/50659 A1) and further in view of Jechoux et al. (US 2002/0041636 A1).

Kim et al. and Eo et al. disclose the claimed limitations as described in paragraph 5 above. Kim et al. and Eo et al. do not disclose the following features: regarding claim 3, wherein the index conversion unit includes multiplication means for multiplying the index (k) with a value of  $SF_{sub,max}/SF$ ; regarding claim 4, wherein said multiplication means includes: a mapping unit for mapping the spreading factor (SF) to a number (s) equal to  $\log_{sub,2}\{SF_{sub,max}/SF\}$ , a shift register adapted to receive and store the index (k) in binary representation, further adapted to receive the number (s) and to shift the stored index (k) by (s) bit positions in the direction of more significant bit positions; regarding claim 14, wherein step a) includes multiplying the index (k) with a value of  $SF_{sub,max}/SF$  and regarding claim 15, wherein said step of multiplying includes the steps of: mapping the spreading factor (SF) to a number (s) equal to  $\log_{sub,2}\{SF_{sub,max}/SF\}$ ; storing the index (k) in binary representation in a shift register; and shifting the stored index (k) by (s) bit positions in the direction of more significant bit positions.

Piccinonno discloses a communication system for orthogonal variable spreading factor and Hadamard matrices generation with the following features: regarding claim 3, wherein the index conversion unit includes multiplication means for multiplying the index (k) with a value of  $SF_{sub,max}/SF$  (Fig. 2, flow chart describing the a spreading sequence generator, see "a generator for rows of Hadamard matrices of dimension SF by an index n of k" recited in lines 21-27 on page 1); regarding claim 4, wherein said multiplication means includes: a mapping unit for mapping the spreading factor (SF) to a number (s) equal to  $\log_{sub,2}\{SF_{max}/SF\}$  (Fig. 2, flow chart describing the a spreading

sequence generator, see "if necessary  $n$  is transformed as described obtaining the binary number" recited in lines 10-14 on page 3); regarding claim 14, wherein step a) includes multiplying the index ( $k$ ) with a value of  $SF_{sub.max}/SF$  (Fig. 2, flow chart describing the a spreading sequence generator, see "a generator for rows of Hadamard matrices of dimension  $SF$  by an index  $n$  of  $k$ " recited in lines 21-27 on page 1) and regarding claim 15, wherein said step of multiplying includes the steps of: mapping the spreading factor ( $SF$ ) to a number ( $s$ ) equal to  $\log_{sub.2}\{SF_{sub.max}/SF\}$  (Fig. 2, flow chart describing the a spreading sequence generator, see "if necessary  $n$  is transformed as described obtaining the binary number" recited in lines 10-14 on page 3).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Kim et al. with Eo et al. by using the features, as taught by Piccinonno, in order to provide wherein the index conversion unit includes multiplication means for multiplying the index ( $k$ ) with a value of  $SF_{sub.max}/SF$  and the multiplication means includes a mapping unit for mapping the spreading factor ( $SF$ ) to a number ( $s$ ) equal to  $\log_{sub.2}\{SF_{sub.max}/SF\}$ . The motivation of using this function is to enhance the system in a cost effective manner.

Kim et al., Eo et al. and Piccinonno do not disclose the following features: regarding claim 4, a shift register adapted to receive and store the index ( $k$ ) in binary representation, further adapted to receive the number ( $s$ ) and to shift the stored index ( $k$ ) by ( $s$ ) bit positions in the direction of more significant bit positions and regarding claim 15, storing the index ( $k$ ) in binary representation in a shift register; and shifting the stored index ( $k$ ) by ( $s$ ) bit positions in the direction of more significant bit positions.

Jechoux et al. disclose a communication system for channel estimation sequence with the following features: regarding claim 4, a shift register adapted to receive and store the index (k) in binary representation (Fig. 3, block diagram discrete in time of the transmission chain between the transmitter and the receiver, see "shift register having l boxes in series referenced by index k" recited in paragraph 0003 lines 6-9), further adapted to receive the number (s) and to shift the stored index (k) by (s) bit positions in the direction of more significant bit positions (Fig. 3, block diagram discrete in time of the transmission chain between the transmitter and the receiver, see "contents slide towards right each time a symbol arrives at the entry" recited in paragraph 0003 lines 9-11) and regarding claim 15, storing the index (k) in binary representation in a shift register (Fig. 3, block diagram discrete in time of the transmission chain between the transmitter and the receiver, see "shift register having l boxes in series referenced by index k" recited in paragraph 0003 lines 6-9); and shifting the stored index (k) by (s) bit positions in the direction of more significant bit positions (Fig. 3, block diagram discrete in time of the transmission chain between the transmitter and the receiver, see "contents slide towards right each time a symbol arrives at the entry" recited in paragraph 0003 lines 9-11).

It would have been obvious to one of the ordinary skill in the art at the time of invention to modify the system of Kim et al. with Eo et al. and Piccinonno by using the features, as taught by Jechoux et al., in order to provide a shift register adapted to receive and store the index (k) in binary representation, further adapted to receive the number (s) and to shift the stored index (k) by (s) bit positions in the direction of more

significant bit positions. The motivation of using this function is to enhance the system in a cost effective manner.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. USP 6,084,884 (Adachi) and US 2003/0072395 A1 (Jia et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed Bokhari whose telephone number is (571) 270-3115. The examiner can normally be reached on Monday through Friday 8:00-17:00 Hrs..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang B. Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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KWANG BIN YAO  
SUPERVISORY PATENT EXAMINER

A handwritten signature in black ink, appearing to read 'Kwong Bin Yao', is written over the printed name and title.